UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,642	08/13/2001	Andrew J. Walker	035905-0103	8019

7590 04/22/2003

Harold C. Wegner
FOLEY & LARDNER
Washington Harbour
3000 K Street, N.W., Suite 500
Washington, DC 20007-5109

EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2829	15

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,642	Applicant(s) WALKER ET AL.	
	Examiner Evan T. Pert	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *13-18,21-24 and 27-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,19,20,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

9,12,14

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 3, 4, 6.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species I in Paper No. 13 is acknowledged. Furthermore, applicant has proposed that Species IV should be examined along with Species I, since the two species comprise related "substrate" and "device" embodiments. Applicant's request for rejoinder and consideration of Species IV along with Species I is granted.

Accordingly, claims 13-18, 21-24 and 27-49 are withdrawn from consideration as being drawn to non-elected Species. Claims 50-68 are withdrawn from consideration being drawn to a non-elected invention (without traverse per item 1 of paper no. 11).

Claims 1-12, 19-20 and 25-26, drawn to Species I and IV, are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 19-20 and 25-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 19-20 and 25-26 recite "at least one driver circuit" which is claimed as being "not located in a bulk monocrystalline silicon substrate" [per independent claim 1].

While a negative limitation can certainly be acceptable at times, applicant's particular use of a negative limitation to claim driver circuit location in this case renders claims indefinite since memory arrays, in general, *inherently* have some kind of "driver circuit" and memory arrays inherently must have this "driver circuit" located *somewhere* (definitively) for a proper understanding of the structure of a memory array device including "at least one driver circuit" [see MPEP 2173.05(i)].

Particularly, to understand the scope of claims 1, 19-20 and 25-26, one of ordinary skill in the art must surmise *everything* suitable that is "not a silicon wafer" to understand the claimed location of "driver circuitry" in the claimed device (with "at least one driver circuit" being inherent to memory array devices in general).

The open-ended claim language with respect to location of "at least one driver" renders claims indefinite since a definitive scope of driver circuit location is not evident from the disclosure. Applicant should positively include limitations drawn to any inventive locations of driver circuits in the claimed 3D memory array, to overcome this rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (U.S. 5,835,396) in view of Wada et al. (Article entitled "Active Body-Bias SOI-CMOS Driver Circuits").

Regarding claim 1, Zhang discloses "a nonvolatile array" (i.e. 3D memory array) comprising "an array of nonvolatile memory devices" (e.g. col. 4, lines 52-54) and at least one driver circuit (i.e. "decoder" per col. 4, line 55) on a "substrate" (10).

Regarding claim 2, Zhang discloses driver circuitry as being located in "semiconductor substrate 10."

Regarding claims 19-20, Zhang discloses "EPROMS" in the array [col. 4, line 54] and that the array is a monolithic three-dimensional array of memory devices [abstract].

Zhang does not disclose the negative limitation that the "semiconductor substrate 10" is "not a bulk monocrystalline silicon substrate." However, Wada et al. teach that their proposed SOI driver circuits (i.e. "not bulk ones") have "excellent speed performance over bulk ones even at large load capacitances" [conclusion] because "SOI devices operate faster and consume less power than bulk ones" [introduction].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to use an SOI substrate (i.e. "not a bulk one") as the "semiconductor substrate 10" disclosed by Zhang for his 3D memory arrays. One of ordinary skill would have been motivated to use SOI for "at least one driver circuit" of Zhang because "SOI devices operate faster and consume less power" [introduction to Wada et al.] and prior art SOI driver circuits "show excellent speed performances over bulk ones" [conclusion to Wada et al.].

Regarding claims 3-12, the examiner takes *Official Notice* that the alternative types of SOI wafers claimed were notoriously well known in the art at the time of the claimed invention (as evident from applicant's lack of particular description of inventive and enabling methodology for forming the various types of SOI wafers claimed).

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt any well known form of SOI substrate as the "semiconductor substrate 10" in Zhang, since all known SOI substrates provide the advantages of "faster" and "less power" as disclosed and taught by Wada et al., specifically for "driver circuitry" such as part of the decoders disclosed by Zhang.

Allowable Subject Matter

5. Claims 25-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose the 3D array of memory devices recited by claims 25-26 corresponding to preferred methodology of manufacture as claimed in U.S. Patent 6,420,215.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
April 18, 2003

EVAN PERT